IN THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. – 18. (Cancelled)

19. (Previously Presented) A semiconductor integrated circuit device comprising:

a first circuit including at least one MOS transistor;

a second circuit to control a frequency of a clock signal to be supplied to the first circuit;

a third circuit to control a supply voltage of the first circuit;

a fourth circuit to control a substrate bias voltage supplied to a semiconductor region where the at least one MOS transistor of the first circuit is formed;

a command generating circuit to generate a first command according to an operating performance of the first circuit; and

a temperature compensation circuit to measure a temperature of the first circuit;

wherein the frequency of the clock signal, the supply voltage and the substrate bias voltage are adjusted according to the operating performance of the first circuit, and

wherein said temperature compensation circuit issues second, third and fourth command signals according to the first command and a temperature of the first circuit measured by the temperature compensation circuit,

the second circuit sets a frequency of the clock signal in response to the second command signal,

the third circuit sets a value of the supply voltage in response to the third command signal, and

the fourth circuit sets a value of the substrate bias voltage in response to the fourth command signal.

20. – 21. (Cancelled)

22. (Previously Presented) A semiconductor integrated circuit device comprising:

a first circuit including at least one MOS transistor;

a second circuit to control a frequency of a clock signal to be supplied to the first circuit;

a third circuit to control a supply voltage of the first circuit; and

a fourth circuit to control a substrate bias voltage supplied to a semiconductor region where the at least one MOS transistor of the first circuit is formed,

wherein the frequency of the clock signal, the supply voltage and the substrate bias voltage are adjusted according to the operating performance of the first circuit, and

wherein the operating performance of the first circuit includes at least an operating speed and a power consumption of the first circuit and the power consumption of the first circuit is controlled according to a remaining quantity of a battery which feeds an electric power to the semiconductor integrated circuit device.

23. (Currently Amended) The semiconductor integrated circuit device according to claim ~~18~~19, wherein the first, second and third command signals generated by the command generating circuit are determined according to at least one of an instruction from an operating system, an instruction from an application software, a signal input from outside of the semiconductor integrated circuit device, a signal from a memory or a processing load of the first circuit.

24. (Currently Amended) The semiconductor integrated circuit device according to claim ~~18~~19, wherein at least one of the command generating circuit, the second circuit, the third circuit, and the fourth circuit is formed on another chip rather than a chip where the first circuit is formed.

25. (Previously Presented) A semiconductor integrated circuit device comprising:

a first circuit including at least one MOS transistor;

a monitor including at least one MOS transistor;

a second circuit to control a frequency of a clock signal to be supplied to the first circuit;

a third circuit to control a supply voltage of the first circuit;

a fourth circuit to control a substrate bias voltage supplied to a semiconductor region where the at least one MOS transistor of said first circuit is formed; and

wherein values of the frequency of the clock signal, the supply voltage and the substrate bias voltage value are set initially in order to satisfy an operating performance of the first circuit,

wherein the clock signal, the supply voltage and the substrate bias voltage are supplied to the monitor, and at least one value of the frequency of the clock signal, the supply voltage and the substrate bias voltage is controlled so as to reduce a delay between an output of the monitor and a reference signal,

wherein the operating performance of the first circuit includes at least an operating speed and a power consumption of the first circuit,

wherein at least one of the frequency of the clock signal, the supply voltage and the substrate bias voltage is initially set in order to satisfy a predetermined value of one of the operating speed and the power consumption of the first circuit; and

wherein at least one of a remaining two values of the frequency of the clock signal, the supply voltage and the substrate bias voltage are initially set in order to improve another of the operating speed and the power consumption of the first circuit.

26. (Previously Presented) The semiconductor integrated circuit device comprising:

a first circuit including at least one MOS transistor;

a monitor including at least one MOS transistor;

a second circuit to control a frequency of a clock signal to be supplied to the first circuit;

a third circuit to control a supply voltage of the first circuit;

a fourth circuit to control a substrate bias voltage supplied to a semiconductor region where the at least one MOS transistor of said first circuit is formed; and

wherein values of the frequency of the clock signal, the supply voltage and the substrate bias voltage value are set initially in order to satisfy an operating performance of the first circuit, based on predetermined combinations of the frequency of the clock signal and the substrate bias voltage according to the supply voltage, and

wherein the clock signal, the supply voltage and the substrate bias voltage are supplied to the monitor, and at least one value of the frequency of the clock signal, the supply voltage and the substrate bias voltage is controlled so as to reduce a delay between an output of the monitor and a reference signal,

a comparator;

wherein the monitor is a delay circuit including inverters connected in series,

wherein the comparator compares an output of the monitor with the reference signal and outputs a first signal when the output of the monitor is later than the reference signal or a second signal when the reference signal is later than the output of the monitor, and

wherein, when the first signal is outputted, the at least one value is controlled so that the operating speed of the first circuit is made faster, and, when the second signal is outputted, the at least one value is controlled so that the operating speed of the first circuit is made lower.

27. – 38. (Cancelled)

39. (New) The semiconductor integrated circuit device according to claim 19,

wherein the fourth circuit applies the substrate bias voltage to the semiconductor region in a range from a forward bias voltage to a reverse bias voltage.

40. (New) The semiconductor integrated circuit device according to claim 22, wherein the frequency of the clock signal, the supply voltage and the substrate bias voltage are determined according to at least one of an instruction from an operating system, an instruction from an application software, a signal input from outside of the semiconductor integrated circuit device, a signal from a memory and a processing load of the first circuit.

41. (New) The semiconductor integrated circuit device according to claim 22,

wherein at least one of the second circuit, the third circuit and the fourth circuit is formed on another chip rather than a chip where the first circuit is formed.

42. (New) The semiconductor integrated circuit device according to claim 22,

wherein the fourth circuit applies the substrate bias voltage to the semiconductor region in a range from a forward bias voltage to a reverse bias voltage.

43. (New) The semiconductor integrated circuit device according to claim 25, wherein the frequency of the clock signal, the supply voltage and the substrate bias voltage are determined according to at least one of an instruction from an operating system, an instruction from an application software, a signal input from outside of the semiconductor integrated circuit device, a signal from a memory or a processing toad of the first circuit.

44. (New) The semiconductor integrated circuit device according to claim 25,

wherein at least one of the second circuit, the third circuit and the fourth circuit is formed on another chip rather than a chip where the first circuit is formed.

45. (New) The semiconductor integrated circuit device according to claim 25,

wherein the fourth circuit applies the substrate bias voltage to the semiconductor region in a range from a forward bias voltage to a reverse bias voltage.

46. (New) The semiconductor integrated circuit device according to claim 26, wherein the frequency of the clock signal, the supply voltage and the substrate

bias voltage are determined according to at least one of an instruction from an operating system, an instruction from an application software, a signal input from outside of the semiconductor integrated circuit device, a signal from a memory or a processing load of the first circuit.

47. (New) The semiconductor integrated circuit device according to claim 26,

wherein at least one of the second circuit, the third circuit and the fourth circuit is formed on another chip rather than a chip where the first circuit is formed.

48. (New) The semiconductor integrated circuit device according to claim 26,

wherein the fourth circuit applies the substrate bias voltage to the semiconductor region in a range from a forward bias voltage to a reverse bias voltage.